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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,718	06/22/2000	Francis G. Celii	TI-29276	8761

7590 02/28/2002  
Jacqueline J Garner  
Texas Instruments Inc  
PO Box 655474  
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Dallas, TX 75265

EXAMINER

BROWN, CHARLOTTE A


ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 02/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

MF-6

<b>Office Action Summary</b>	Application No. <b>09/599,718</b>	Applicant(s) <b>Kraft et al.</b>	
	Examiner <b>Charlotte A. Brown</b>	Art Unit <b>1765</b>	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on Dec 18, 2001
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some\* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

- |  |  |
|--|--|
| 15) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                   | 18) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 16) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)          | 19) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 17) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ | 20) <input type="checkbox"/> Other:  |

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### DETAILED ACTION

1. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.
2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (US 6,019,906) in view of Grill et al. (US 6,140,226).

Jang teaches a hard masking method for forming a patterned microelectronics layer within a microelectronics fabrication. A semiconductor substrate is provided. A blanket first dielectric layer is formed on the semiconductor substrate. The dielectric layer may be formed from any of several dielectric materials that are conventional in the art (Column 10, lines 46-50). This reads on the applicant's limitation of forming an interlevel dielectric layer over a semiconductor body. Patterned conductor layers are formed over the blanket first dielectric layer. A blanket inter-metal dielectric layer is formed over the substrate. The layer is formed from an oxygen containing plasma etchable material which is a low dielectric constant material. The materials may include but are not limited to organic polymer spin-on-polymer dielectric materials (Column 11, lines 32-

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50). A hard mask layer is formed over the structure. A series of patterned photoresist layers are formed (Column 12, lines 12-30). This reads on the applicant's limitation of forming a via pattern over the hard mask. A first plasma etch is employed to etch through the hard mask layer (Column 12, lines 51-57). A second plasma etch is performed to etch the blanket inter-metal dielectric layer (Column 13, lines 7-20). This reads on the applicant's limitation of extending the via by selectively etching the intrametal dielectric layer.

Unlike the claimed invention, Jang does not teach methods for depositing a BARC layer over the hard mask and within the via, forming a trench pattern over the BARC layer, and etching a trench in the intrametal dielectric layer.

Grill discloses a dual damascene process. A thin layer of conductive or insulating material is deposited over a hardmask and in a via. Possible conductive and insulating materials include TaN, TiN, and HfN (Column 5, lines 43-61). Titanium nitride (TiN) is a BARC layer (See Padmanaban et al. , Column 2, lines 1-3). This reads on the applicant's limitation of depositing a BARC layer over the hardmask within the via. A trench pattern is formed over the BARC layer (Figure 3F). A trench is etched in the dielectric layer. Portions of the BARC layer are then removed before fabrication of any overlying wiring or via levels (Column 6, lines 6-14).

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Jang with the methods of depositing a BARC layer over the hard mask and within the via, forming a trench pattern over the BARC layer, and etching a trench in the

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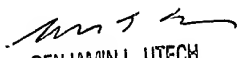
intrametal dielectric layer as taught by Grill. These additional steps would have been anticipated in order to form a trench in the intrametal dielectric layer.

4. Any inquiry concerning this communication from the Examiner should be directed to Charlotte A. Brown whose telephone number is (703) 305-0727. The Examiner can normally be reached during the hours of 9:00AM to 6:30PM.

The fax phone numbers where this application or proceeding is assigned are 703-305-4508 for regular communications and 703-872-9311 for After Final communications.

CAB

February 22, 2002

  
BENJAMIN L. UTECH  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 1700